



remative Specification
Preliminary Specification
Approval Specification

MODEL NO.: V460HK1 **SUFFIX: PS1**

Customer:	
APPROVED BY	SIGNATURE
Name / Title Note	
Please return 1 copy for your signature and comments.	confirmation with your

Approved By	Checked By	Prepared By
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Date: 26 Apr. 2011 Version 1.0





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REVISION HISTORY

Apr. 26, 2011	A II		
		All	The preliminary specification was first issued.

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1. GENERAL DESCRIPTION

Global LCD Panel Exchange Center

1.1 OVERVIEW

V460HK1-PS1 is a 46" TFT Liquid Crystal Display product with driver ICs and 4ch-LVDS interface. This product supports 1920 x 1080 Full HDTV format and can display 1.07G (8-bit+Hi-FRC)colors. The backlight unit is not built

1.2 FEATURES

CHARACTERISTICS ITEMS	SPECIFICATIONS
Screen Diagonal [in]	46
Pixels [lines]	1920 × 1080
Active Area [mm]	1018.08(H) × 572.67(V) (46" diagonal)
Sub-Pixel Pitch [mm]	0.17675(H) × 0.53025(V)
Pixel Arrangement	RGB vertical stripe
Weight [g]	TYP. 2500g
Physical Size [mm]	1049.48(H) × 627.37(V) × 1.78(D) Typ.
Display Mode	Transmissive mode / Normally black
Contract Datio	6500:1 Typ.
Contrast Ratio	(Typical value measure at CMI's module)
Glass thickness (Array / CF) [mm]	0.7 / 0.7
Viouing Angle (CP, 20)	+88/-88(H), +88/-88(V) Typ. (CR≥20)
Viewing Angle (CR>20)	(Typical value measure at CMI's module)
	Rc = (0.650, 0.325)
	Gc = (0.265, 0.570)
Color Chromaticity	Bc = (0.131, 0.122)
	Wc= (0.297, 0.344)
	* Please refer to "color chromaticity" on p.24
Cell Transparency [%]	4.8%
Polarizer Surface Treatment	Super Wide View Glare coating, Hard coating (3H)

1.3 MECHANICAL SPECIFICATIONS

Item	Min.	Тур.	Max.	Unit	Note
Weight		2500		g	-
I/F connector mounting position	The mounting incli screen center with			51.75/22.25	(1)(2)

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

Note (2) Connector mounting position



PRODUCT SPECIFICATION

2. ABSOLUTE MAXIMUM RATINGS

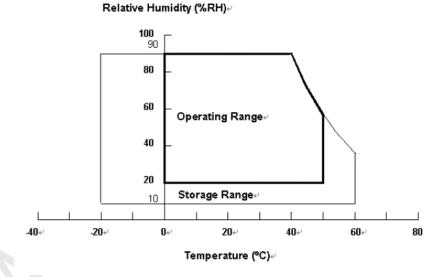
2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Va	lue	Unit	Note	
item	Symbol	Min.	Max.	5111		
Storage Temperature	TST	-20	+60	ºC	(1)	
Operating Ambient Temperature	TOP	0	50	ºC	(1), (2)	

Note (1) Temperature and relative humidity range is shown in the figure below.

- (a) 90 %RH Max. (Ta \leq 40 ${}^{\circ}$ C).
- (b) Wet-bulb temperature should be 39 °C Max. (Ta > 40 °C).
- (c) No condensation.

Note (2) The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 65 °C with LCD module alone in a temperature controlled chamber. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 65 °C. The range of operating temperature may degrade in case of improper thermal management in final product design.





2.2 PACKAGE STORAGE

When storing modules as spares for a long time, the following precaution is necessary.

- (a) Do not leave the module in high temperature, and high humidity for a long time, It is highly recommended to store the module with temperature from 0 to 35 $^{\circ}$ C at normal humidity without condensation.
- (b) The module shall be stored in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.

2.3 ELECTRICAL ABSOLUTE RATINGS

Item	Symbol	Value		Unit	Note	
item	Syllibol	Min.	Max.	Offic	Note	
Power Supply Voltage	VCC	-0.3	13.5	V	(1)	
Logic Input Voltage	VIN	-0.3	3.6	V	(1)	

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.





3. ELECTRICAL CHARACTERISTICS

3.1 TFT LCD MODULE

 $(Ta = 25 \pm 2 \,{}^{\circ}C)$

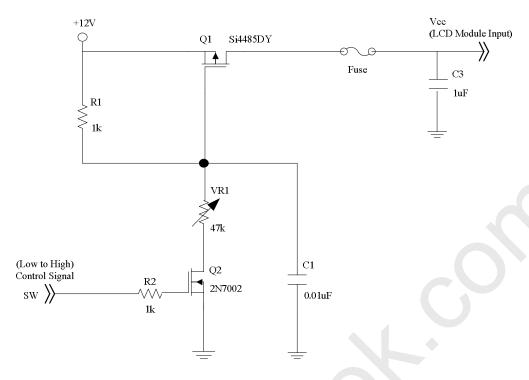
	Parameter S		Symbol	Value			Unit	Note
	Parameter			Min.	Тур.	Max.	Offic	note
Power Sup	Power Supply Voltage		V _{CC}	10.8	12	13.2	V	(1)
Rush Curr	ent		I _{RUSH}	_	_	4.55	Α	(2)
		White Pattern	_	_	0.58	_	Α	
Power Sup	oply Current	Horizontal Stripe	_	_	1.3	1.37	А	(3)
	Black Pa		_	_	0.58		Α	
	Differential Input High Threshold Voltage		V _{LVTH}	+100	_		mV	
	Differential Input Low Threshold Voltage		V _{LVTL}	_		-100	mV	
LVDS interface	Common Input Voltage		V _{CM}	1.0	1.2	1.4	V	(4)
	Differential in	Differential input voltage		200		600	mV	
	Terminating Resistor		R _T		100	_	ohm	
CMOS	Input High T	hreshold Voltage	V _{IH}	2.7	_	3.3	V	
interface	Input Low Threshold Voltage		V _{IL}	0	_	0.7	V	

Note (1) The module should be always operated within the above ranges.

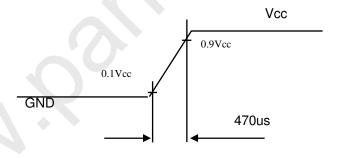
Note (2) Measurement condition:







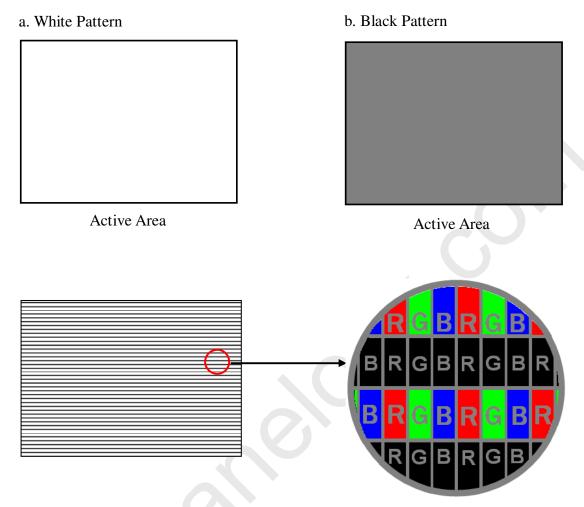
Vcc rising time is 470us



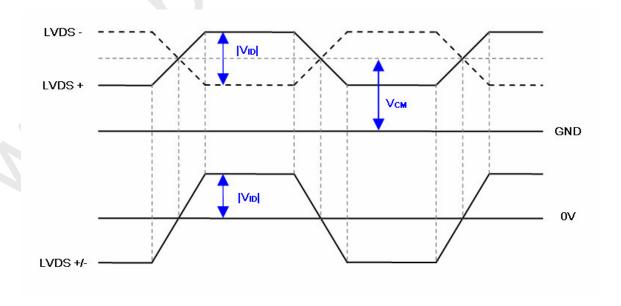


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Note (3) The specified power supply current is under the conditions at Vcc = 12 V, Ta = 25 \pm 2 $^{\circ}$ C, f_v = 120 Hz, whereas a power dissipation check pattern below is displayed.



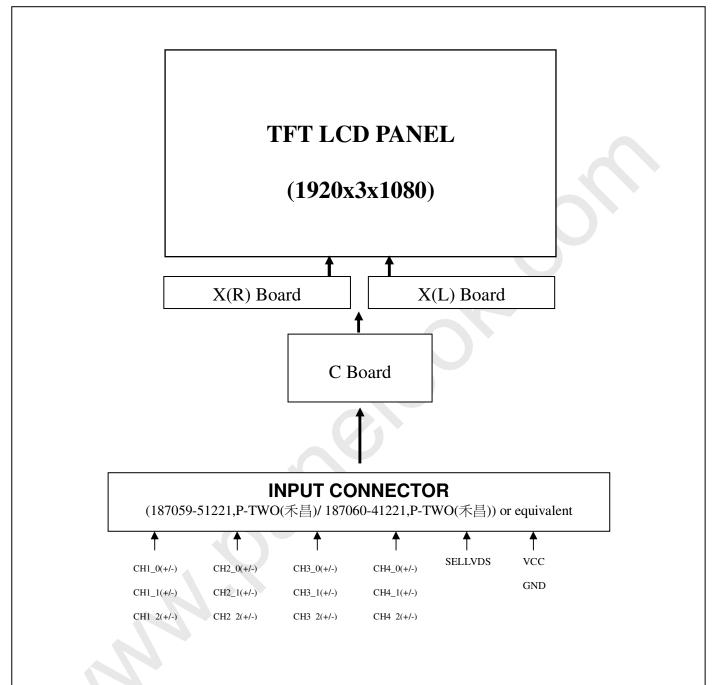
Note (4) The LVDS input characteristics are as follows:





4. BLOCK DIAGRAM OF INTERFACE

4.1 TFT LCD MODULE







5. INPUT TERMINAL PIN ASSIGNMENT

5.1 TFT LCD Module Input

CNF1 Connector Pin Assignment (187059-51221,P-TWO(禾昌) or equivalent)

Pin	Name	Description	Note
1	GND	Ground	
2	N.C.	No Connection	(1)
3	N.C.	No Connection	(1)
4	N.C.	No Connection	(1)
5	N.C.	No Connection	(1)
6	N.C.	No Connection	(1)
7	SELLVDS	LVDS Data Format Selection	(2)
8	N.C.	No Connection	(1)
9	N.C.	No Connection	(1)
10	N.C.	No Connection	(1)
11	GND	Ground	
12	CH1[0]-	First pixel Negative LVDS differential data input. Pair 0	
13	CH1[0]+	First pixel Positive LVDS differential data input. Pair 0	
14	CH1[1]-	First pixel Negative LVDS differential data input. Pair 1	
15	CH1[1]+	First pixel Positive LVDS differential data input. Pair 1	
16	CH1[2]-	First pixel Negative LVDS differential data input. Pair 12	
17	CH1[2]+	First pixel Positive LVDS differential data input. Pair 2	
18	GND	Ground	
19	CH1CLK-	First pixel Negative LVDS differential clock input.	
20	CH1CLK+	First pixel Positive LVDS differential clock input.	
21	GND	Ground	
22	CH1[3]-	First pixel Negative LVDS differential data input. Pair 3	
23	CH1[3]+	First pixel Positive LVDS differential data input. Pair 3	
24	CH1[4]-	First pixel Negative LVDS differential data input. Pair 4	
25	CH1[4]+	First pixel Positive LVDS differential data input. Pair 4	
26	N.C.	No Connection	(1)
27	N.C.	No Connection	(1)
28	CH2[0]-	Second pixel Negative LVDS differential data input. Pair 0	

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29	CH2[0]+	Second pixel Positive LVDS differential data input. Pair 0	
30	CH2[1]-	Second pixel Negative LVDS differential data input. Pair 1	
31	CH2[1]+	Second pixel Positive LVDS differential data input. Pair 1	
32	CH2[2]-	Second pixel Negative LVDS differential data input. Pair 2	
33	CH2[2]+	Second pixel Positive LVDS differential data input. Pair 2	
34	GND	Ground	
35	CH2CLK-	Second pixel Negative LVDS differential clock input.	
36	CH2CLK+	Second pixel Positive LVDS differential clock input.	
37	GND	Ground	
38	CH2[3]-	Second pixel Negative LVDS differential data input. Pair 3	
39	CH2[3]+	Second pixel Positive LVDS differential data input. Pair 3	
40	CH2[4]-	Second pixel Negative LVDS differential data input. Pair 4	
41	CH2[4]+	Second pixel Positive LVDS differential data input. Pair 4	
42	N.C.	No Connection	(1)
43	N.C.	No Connection	(1)
44	GND	Ground	
45	GND	Ground	
46	GND	Ground	
47	N.C.	No Connection	(1)
48	VCC	+12V power supply	
49	VCC	+12V power supply	
50	VCC	+12V power supply	
	VICC	1037	

CNF2 Connector Pin Assignment (187060-41221,P-TWO(禾昌) or equivalent)

Pin	Name	Description	Note
1	GND	Ground	
2	N.C.	No Connection	(1)
3	N.C.	No Connection	(1)
4	N.C.	No Connection	(1)
5	N.C.	No Connection	(1)





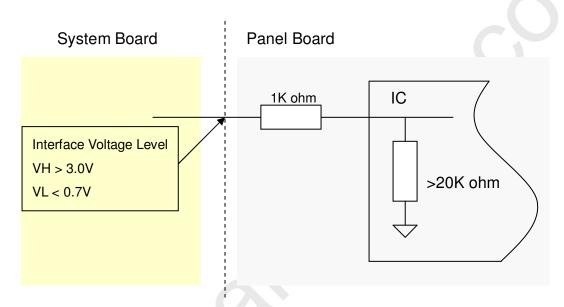
7 N 8 N 9 G 10 C	N.C. N.C. GND	No Connection No Connection No Connection Ground	(1) (1) (1)
8 N 9 G 10 C	N.C. GND CH3[0]-	No Connection Ground	<u> </u>
9 G	GND CH3[0]-	Ground	(1)
10 C	CH3[0]-		
11 C		Third : 1N .: INDO 1:00 .: 111 .: D : 0	
	CH3[0]+	Third pixel Negative LVDS differential data input. Pair 0	
12 (Third pixel Positive LVDS differential data input. Pair 0	
12	CH3[1]-	Third pixel Negative LVDS differential data input. Pair 1	-
13 C	CH3[1]+	Third pixel Positive LVDS differential data input. Pair 1	
14 C	CH3[2]-	Third pixel Negative LVDS differential data input. Pair 2	
15 C	CH3[2]+	Third pixel Positive LVDS differential data input. Pair 2	
16 G	GND	Ground	
17 C	CH3CLK-	Third pixel Negative LVDS differential clock input.	
18 C	CH3CLK+	Third pixel Positive LVDS differential clock input.	
19 G	GND	Ground	
20 C	CH3[3]-	Third pixel Negative LVDS differential data input. Pair 3	
21 C	CH3[3]+	Third pixel Positive LVDS differential data input. Pair 3	
22 C	CH3[4]-	Third pixel Negative LVDS differential data input. Pair 4	
23 C	CH3[4]+	Third pixel Positive LVDS differential data input. Pair 4	
24 N	N.C.	No Connection	(1)
25 N	N.C.	No Connection	(1)
26 C	CH4[0]-	Fourth pixel Negative LVDS differential data input. Pair 0	
27 C	CH4[0]+	Fourth pixel Positive LVDS differential data input. Pair 0	
28 C	CH4[1]-	Fourth pixel Negative LVDS differential data input. Pair 1	
29 C	CH4[1]+	Fourth pixel Positive LVDS differential data input. Pair 1	
30 C	CH4[2]-	Fourth pixel Negative LVDS differential data input. Pair 2	
31 C	CH4[2]+	Fourth pixel Positive LVDS differential data input. Pair 2	
32 G	GND	Ground	
33 C	CH4CLK-	Fourth pixel Negative LVDS differential clock input.	
34 C	CH4CLK+	Fourth pixel Positive LVDS differential clock input.	
35 G	GND	Ground	
36 C	CH4[3]-	Fourth pixel Negative LVDS differential data input. Pair 3	
37 C	CH4[3]+	Fourth pixel Positive LVDS differential data input. Pair 3	





38	CH4[4]-	Fourth pixel Negative LVDS differential data input. Pair 4	
39	CH4[4]+	Fourth pixel Positive LVDS differential data input. Pair 4	
40	N.C.	No Connection	(1)
41	N.C.	No Connection	(1)

- Note (1) Reserved for internal use. Please leave it open.
- Note (2) High=connect to +3.3V: JEIDA Format ; Low= connect to GND or Open: VESA Format.
- Note (3) Interface optional pin has internal scheme as following diagram. Customer should keep the interface voltage level requirement as below.

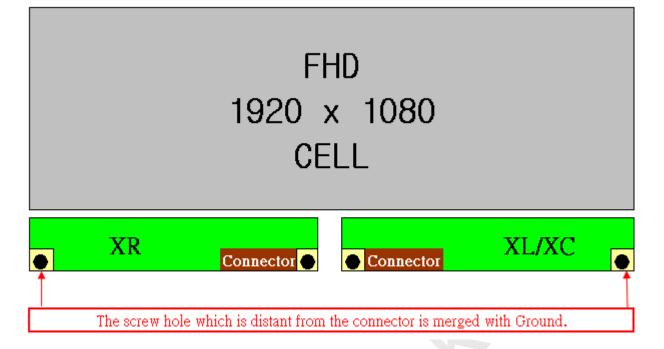


Note (4) LVDS 4-port Data Mapping

Port	Channel of LVDS	Data Stream
1st Port	First Pixel	1, 5, 9,1913, 1917
2nd Port	Second Pixel	2, 6, 10,1914, 1918
3rd Port	Third Pixel	3, 7, 11,1915, 1919
4th Port	Fourth Pixel	4, 8, 12,1916, 1920







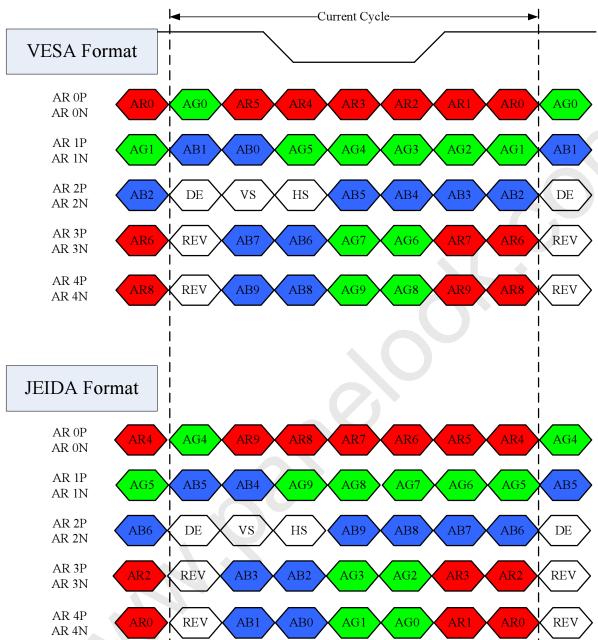




5.2 LVDS INTERFACE

VESA Format : SELLVDS = L or Open

JEIDA Format : SELLVDS = H



AR0~AR9: First Pixel R Data (9; MSB, 0; LSB)

AG0~AG9: First Pixel G Data (9; MSB, 0; LSB) AB0~AB9: First Pixel B Data (9; MSB, 0; LSB)

DE : Data enable signal
DCLK : Data clock signal

RSV: Reserved





5.3 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 10-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of the color versus

da	ta input.																														
)ata	Sign	al													
	Color					Re	ed									Gre	een									ВІ	ue				
		R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0	В9	B8	В7	В6	B5	B4	ВЗ	B2	B1	В0
	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
Basic	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
Colors	Cyan	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Red (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1)	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of	Red (2)	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:			:	:	:	:	:	:	:	:	:(:	:		:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:			:	:	:	:	:	:	:			:	÷	:	:	:	:	:	:	:	;	:	:	:	:	:	:	:	:	:
	Red (1021)	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ried	Red (1022)	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1023)	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
Gray	Green (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
Scale	:		:	. :	÷	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
Of	:		:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
Green	Green (1021)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0
areen	Green (1022)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
	Green (1023)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	Blue (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray	Blue (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
Of	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
Blue	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue (1021)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1

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Blue (1022)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0
Blue (1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1

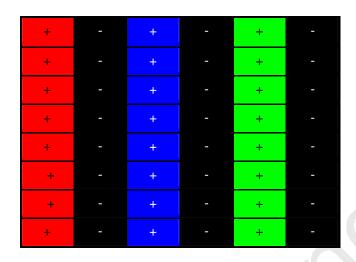
Note (1) 0: Low Level Voltage, 1: High Level Voltage

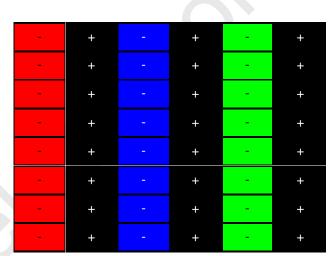
5.4 FLICKER (V-com) ADJUSTMENT

(1) Adjustment Pattern:

Column-inversion pattern was shown as below. If customer need below pattern, please directly contact with Account FAE.

Frame N Frame N+1





(2) Adjustment method: (Digital V-com)

Programmable memory IC is used for Digital V-com adjustment in this model. CMI provide Auto V-com tools to adjust Digital V-com. The detail connection and setting instruction, please directly contact with Account FAE or refer CMI Auto V-com adjustment OI. Below items is suggested to be ready before Digital V-com adjustment in customer LCM line.





PRODUCT SPECIFICATION

6. INTERFACE TIMING

6.1 INPUT SIGNAL TIMING SPECIFICATIONS

 $(Ta = 25 \pm 2 \, {}^{\circ}C)$

The input signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Тур.	Max.	Unit	Note
	Frequency	F _{clkin} (=1/TC)	60	74.25	80	MHz	
LVDS Receiver	Input cycle to cycle jitter	T _{rcl}	_	_	200	ps	(3)
Clock	Spread spectrum modulation range	Fclkin_mo	F _{clkin} -2%	_	F _{clkin} +2%	MHz	(4)
	Spread spectrum modulation frequency	F _{SSM}			200	KHz	(4)
LVDS	Setup Time	Tlvsu	600	- <	- •	ps	
Receiver Data	Hold Time	Tlvhd	600		-	ps	(5)
	Frame Rate	F _{r5}	_	100	_	Hz	
Vertical	Traine riate	F _{r6}	1	120	_	Hz	
Active Display	Total	Tv	1115	1125	1135	Th	Tv=Tvd+Tv b
Term	Display	Tvd	1080	1080	1080	Th	_
	Blank	Tvb	35	45	55	Th	_
Horizontal Active	Total	Th	540	550	575	Tc	Th=Thd+T
Display	Display	Thd	480	480	480	Тс	_
Term	Blank	Thb	60	70	95	Тс	_

Note (1) Since the module is operated in DE only mode, Hsync and Vsync input signals should be set to low logic level. Otherwise, this module would operate abnormally.

Note (2) Please make sure the range of pixel clock has follow the below equation:

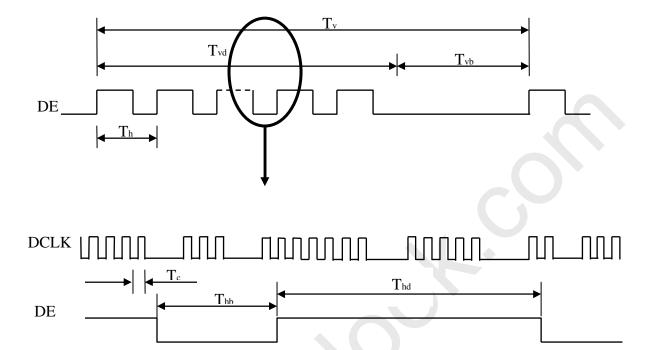
$$\begin{aligned} & \text{Fclkin(max)} \ge \text{Fr6} \times \text{Tv} \times \text{Th} \\ & \text{Fr5} \times \text{Tv} \times \text{Th} \ge \text{Fclkin(min)} \end{aligned}$$



DAT

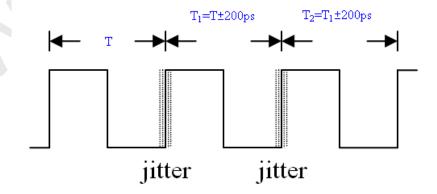
PRODUCT SPECIFICATION

INPUT SIGNAL TIMING DIAGRAM



Valid display data (960 clocks)

Note (3) The input clock cycle-to-cycle jitter is defined as below figures. Trcl = $IT_1 - TI$

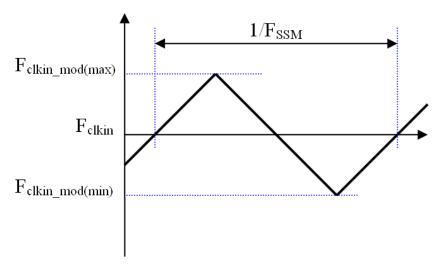






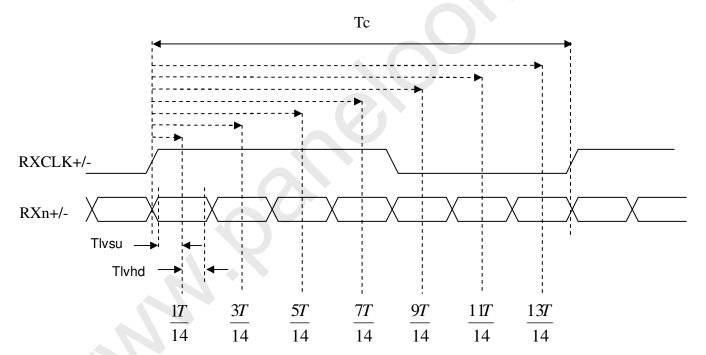
PRODUCT SPECIFICATION

Note (4) The SSCG (Spread spectrum clock generator) is defined as below figures.



Note (5) The LVDS timing diagram and setup/hold time is defined and showing as the following figures.

LVDS RECEIVER INTERFACE TIMING DIAGRAM



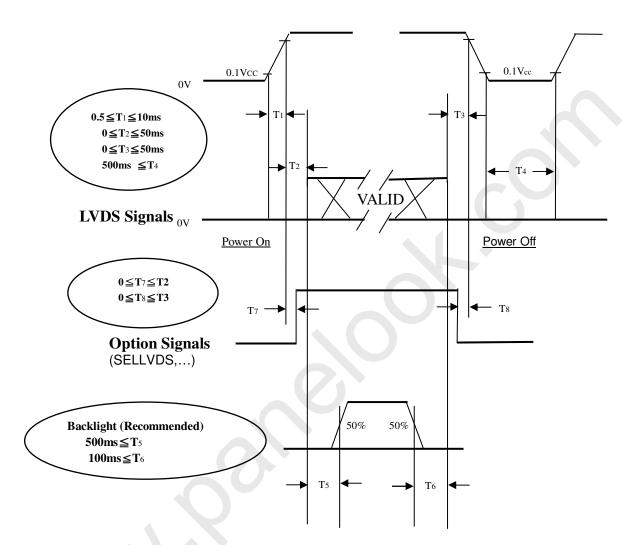


6.2 POWER ON/OFF SEQUENCE

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 $(Ta = 25 \pm 2 \,{}^{\circ}C)$

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should be as the diagram below.



Power ON/OFF Sequence

- Note (1) The supply voltage of the external system for the module input should follow the definition of Vcc.
- Note (2) Apply the lamp voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.
- Note (3) In case of Vcc is in off level, please keep the level of input signals on the low or high impedance. If T2<0,that maybe cause electrical overstress failure.
- Note (4) T4 should be measured after the module has been fully discharged between power off and on period.
- Note (5) Interface signal shall not be kept at high impedance when the power is on.





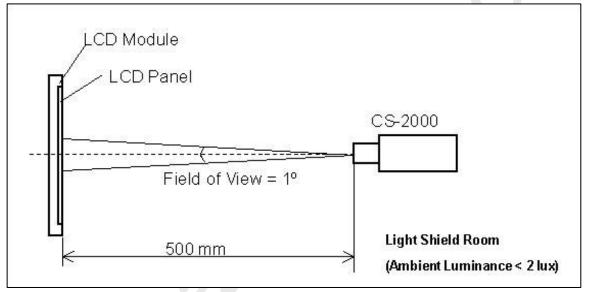
PRODUCT SPECIFICATION

7. OPTICAL CHARACTERISTICS

7.1 TEST CONDITIONS

Item	Symbol	Value	Unit			
Ambient Temperature	Ta	25±2	°C			
Ambient Humidity	На	50±10	%RH			
Supply Voltage	V _{CC}	12.0	V			
Input Signal	According to typical va	alue in "3. ELECTRICAL (CHARACTERISTICS"			
LED Current	IL	120	mA			
Vertical Frame Rate	Fr	120	Hz			

The LCD module should be stabilized at given temperature for 1 hour to avoid abrupt temperature change during measuring in a windless room.







7.2 OPTICAL SPECIFICATIONS

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The relative measurement methods of optical characteristics are shown as below. The following items should be measured under the test conditions described in 7.1 and stable environment shown in 7.1.

lte	em	Symbol	Condition	Min.	Тур.	Max.	Unit	Note
	Red	Rcx			0.650		-	
	neu	Rcy			0.325		-	
	Green	Gcx	$\theta_x=0^\circ, \theta_Y=0^\circ$		0.265		-	
Color	Green	Gcy	Viewing Angle at Normal		0.570		-	(0) (5)
Chromaticit	y Blue	Всх	Direction	-	0.131	-	-	(0),(5)
	Blue	Всу	Standard light source "C"		0.122		-	
	White	Wcx			0.297		-	
	vvriite	Wcy			0.344		-	
Center Tran	smittance	T%	$\theta_x=0^\circ, \theta_Y=0^\circ$	ı	4.8	ı	%	(1),(7)
Contrast Ra	ntio	CR	with CMI module		6500	ı	ı	(1),(3)
Response 1	īme	Gray to gray	θ_x =0°, θ_Y =0° with CMI Module@60Hz	-	5.5			(1),(4)
White Varia	tion	δW	θ_{x} =0°, θ_{Y} =0° with CMI module	-	-	1.3	-	(1),(6)
	Horizontal	θ_{x} +			88			
Viewing	nonzoniai	θ _x -	CR≥20		88		Dog	(1) (2)
Angle	Vertical	θ_{Y} +	with CMI module		88		Deg.	(1),(2)
	vertical	θγ-			88			

Note (0) Light source is the standard light source "C" which is defined by CIE and driving voltage are based on suitable gamma voltages. The calculating method is as following:

- 1. Measure Module's W,R,G,B spectrum and BLU's spectrum. Which BLU (for V460H1-LE3) is supplied by CMI.
- 2. Calculate cell's spectrum.
- 3. Calculate cell's chromaticity by using the spectrum of standard light source "C".

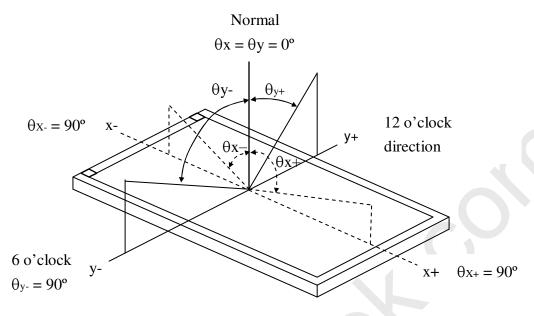
Note (1) Light source is the BLU which supplied by CMI and driving voltage are based on suitable gamma voltages.



PRODUCT SPECIFICATION

Note (2) Definition of Viewing Angle (θx , θy):

Viewing angles are measured by Autronic Conoscope Cono-80 (or Eldim EZ-Contrast 160R)



Note (3) Definition of Contrast Ratio (CR):

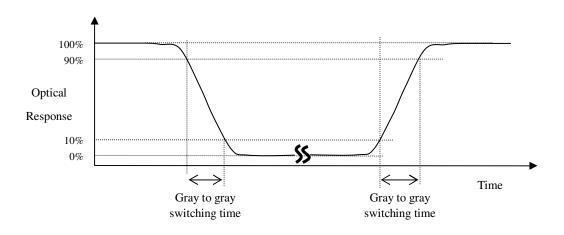
The contrast ratio can be calculated by the following expression.

L255: Luminance of gray level 1023

L 0: Luminance of gray level 0

CR = CR (5), where CR (X) is corresponding to the Contrast Ratio of the point X at the figure in Note (6).

Note (4) Definition of Gray-to-Gray Switching Time:

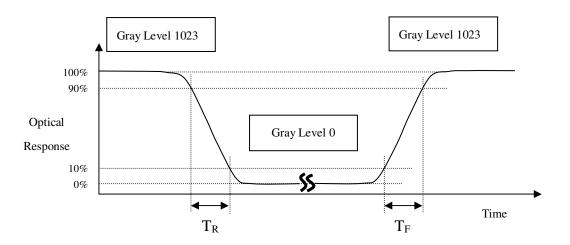


The driving signal means the signal of gray level 0, 124, 252, 380, 508, 636, 764, 892 and 1023. Gray to gray average time means the average switching time of gray level 0, 124, 252, 380, 508, 636, 764, 892 and 1023 to each other.



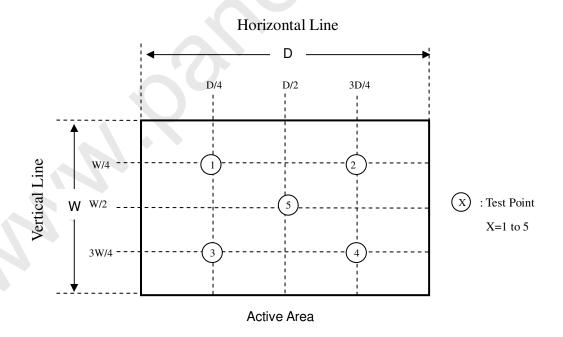


Note (5) Definition of Response Time (T_R , T_F):



Note (6) Definition of White Variation (δW):

Measure the luminance of gray level 1023 at 5 points $\delta W = \text{Maximum } [L\ (1), L\ (2), L\ (3), L\ (4), L\ (5)] \ / \ \text{Minimum } [L\ (1), L\ (2), L\ (3), L\ (4), L\ (5)]$ where L (X) is corresponding to the luminance of the point X at the figure below.







Note (7) Definition of Transmittance (T%):

Measure the luminance of gray level 1023 at center point of LCD module.

$$\label{eq:Transmittance} Transmittance \; (T\%) = \frac{\text{Luminance of LCD module}}{\text{Luminance of backligh unit}} \times 100\% \; \text{PRECAUTIONS}$$

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Global LCD Panel Exchange Center

PRODUCT SPECIFICATION

8. PRECAUTIONS

8.1 ASSEMBLY AND HANDLING PRECAUTIONS

- Do not apply rough force such as bending or twisting to the module during assembly.
- It is recommended to assemble or to install a module into the user's system in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.
- [3] Do not apply pressure or impulse to the module to prevent the damage of LCD panel and Backlight.
- [4] Always follow the correct power-on sequence when the LCD module is turned on. This can prevent the damage and latch-up of the CMOS LSI chips.
- [5] The distance between COF edge and rib of BLU must bigger than 5mm. This can prevent the damage of COF when assemble the module.
- [6] Do not design sharp-pointed structure / parting line / tooling gate on the COF position of plastic parts, because the burr will scrape the COF.
- [7] If COF would bended to assemble in the module. Do not put the IC location on the bending corner of COF.
- [8] The gap between COF IC and any structure of BLU must bigger than 2mm. This can prevent the damage of COF IC
- [9] Bezel opening must have no burr. Burr will scrape the panel surface.
- [10] Bezel of module and bezel of set can not press or touch the panel surface. It will make light leakage or scrape.
- [11] When module used FFC / FPC, but no FFC / FPC to be attached in the open cell. Customer can refer the FFC / FPC drawing and buy it by self.
- [12] The gap between Panel and any structure of Bezel must bigger than 2mm. This can prevent the damage of Panel.
- [13] Do not plug in or pull out the I/F connector while the module is in operation.
- [14] Do not disassemble the module.
- [15] Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.
- [16] Moisture can easily penetrate into LCD module and may cause the damage during operation.
- [17] When storing modules as spares for a long time, the following precaution is necessary.
 - [17.1] Do not leave the module in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35°C at normal humidity without condensation.
 - [17.2] The module shall be stored in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.
- [18] When ambient temperature is lower than 10°C, the display quality might be reduced.

8.2 SAFETY PRECAUTIONS

Version 1.0

- [1] The startup voltage of a Backlight is approximately 1000 Volts. It may cause an electrical shock while assembling with the inverter. Do not disassemble the module or insert anything into the Backlight unit.
- [2] If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of





contact with hands, skin or clothes, it has to be washed away thoroughly with soap.

After the module's end of life, it is not harmful in case of normal operation and storage.

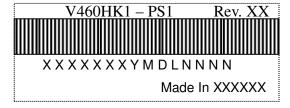




9. DEFINITION OF LABELS

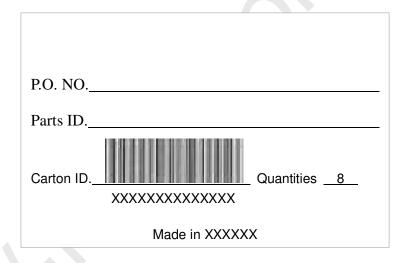
9.1 CMI OPEN CELL LABEL

The barcode nameplate is pasted on each open cell as illustration for CMI internal control.



9.2 CARTON LABEL

The barcode nameplate is pasted on each box as illustration, and its definitions are as following explanation



(a) Model Name: V460HK1- PS1(b) Carton ID: CMI internal control

(c) Quantities: 8



PRODUCT SPECIFICATION

10. PACKAGING

10.1 PACKAGING SPECIFICATIONS

- (1) 8 LCD TV PANELS / 1 BOX
- (2) BOX DIMENSIONS :1238 (L) X 842 (W) X 240(H)
- (3) WEIGHT: APPROXIMATELY 38KG (8 PANELS PER BOX)

10.2 PACKAGING METHOD

Figures 10-1 and 10-2 are the packing method

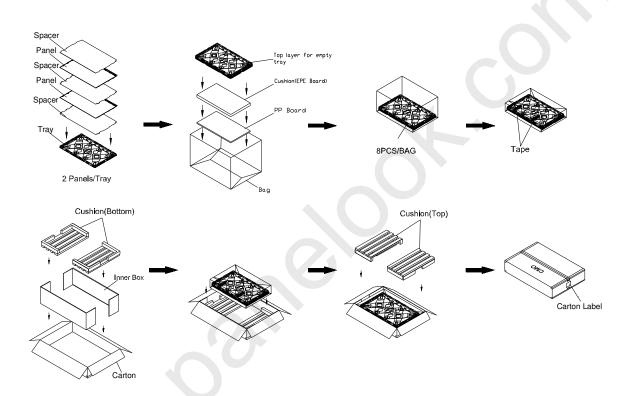


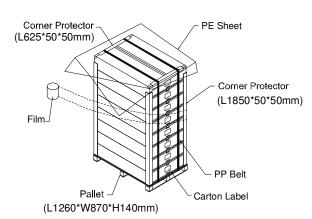
Figure.10-1 packing method





PRODUCT SPECIFICATION

Sea & Land Transportation



Air Transportation

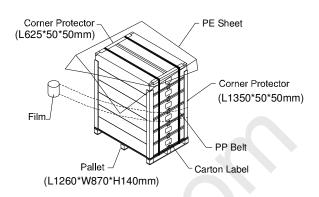


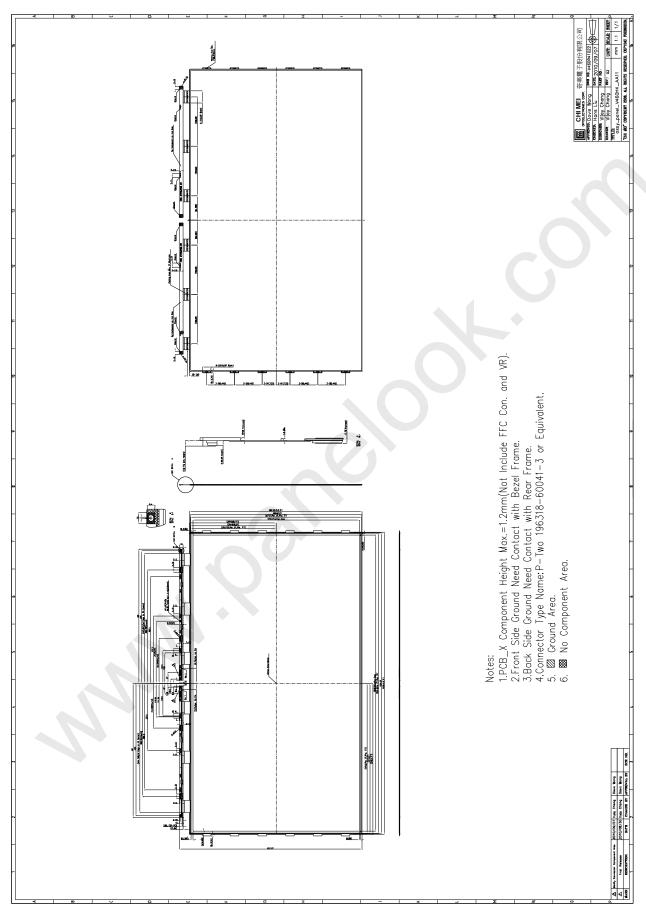
Figure.10-2 packing method





PRODUCT SPECIFICATION

11. MECHANICAL CHARACTERISTIC



Version 1.0 Date: 26 Apr. 2011

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